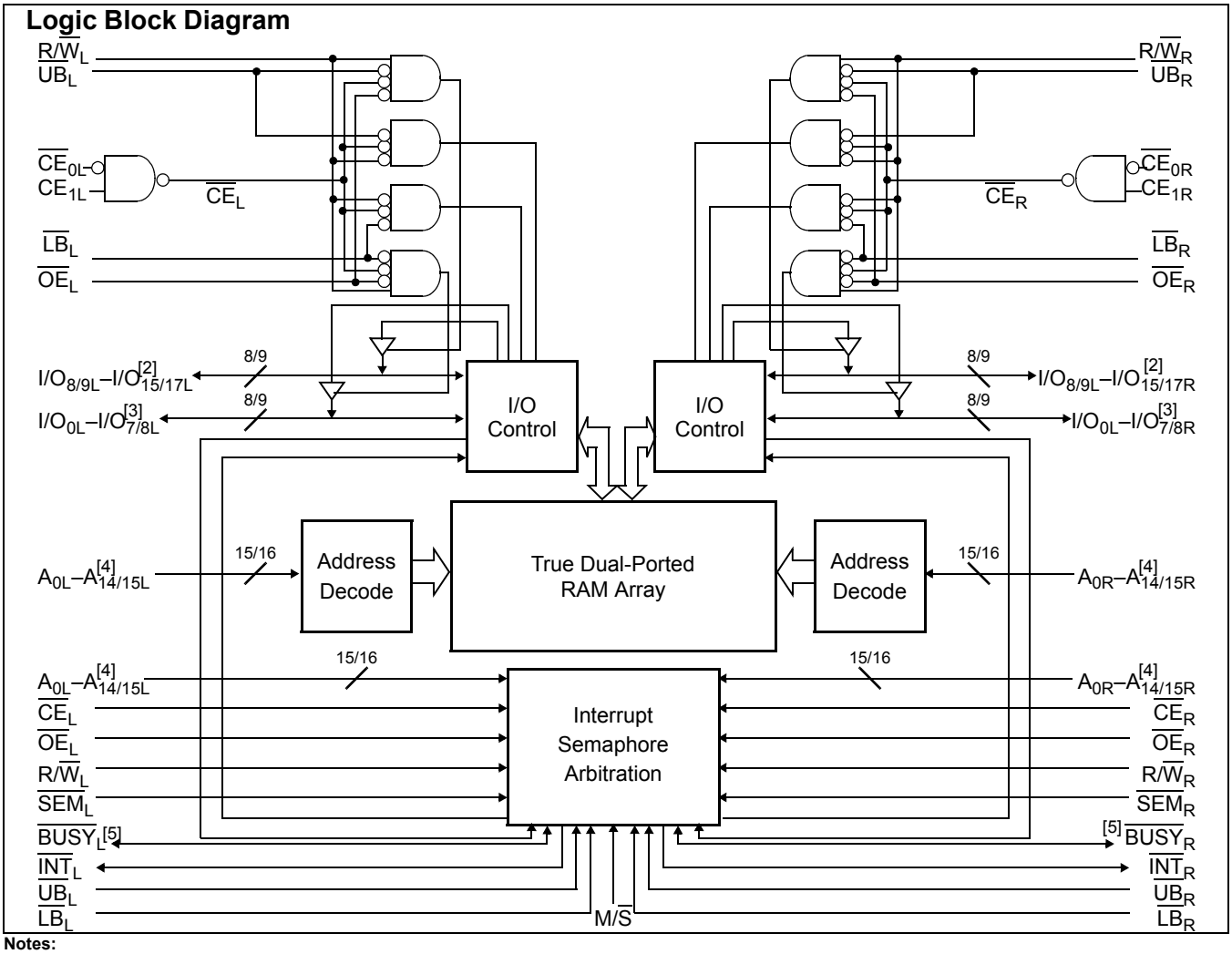
CY7C027/028
CY7C037/038

32K/64K x 16/18 Dual-Port Static RAM

Features

- True Dual-Ported memory cells which allow simultaneous access of the same memory location
- 32K x 16 organization (CY7C027)
- 64K x 16 organization (CY7C028)
- 32K x 18 organization (CY7C037)
- 64K x 18 organization (CY7C038)
- 0.35-micron CMOS for optimum speed/power
- High-speed access: 12[1]/15/20 ns
- Low operating power
  - Active: I_{CC} = 180 mA (typical)
  - Standby: I_{SB3} = 0.05 mA (typical)
- Fully asynchronous operation
- Automatic power-down
- Expandable data bus to 32/36 bits or more using Master/Slave chip select when using more than one device
- On-chip arbitration logic
- Semaphores included to permit software handshaking between ports
- $\overline{INT}$ flags for port-to-port communication
- Separate upper-byte and lower-byte control
- Dual Chip Enables
- Pin select for Master or Slave
- Commercial and industrial temperature ranges
- Available in 100-pin TQFP
- Pb-Free packages available

Logic Block Diagram



Notes:
1. See page 6 for Load Conditions.
2. I/O_8–I/O_{15} for x16 devices; I/O_9–I/O_{17} for x18 devices.
3. I/O_0–I/O_7 for x16 devices; I/O_0–I/O_8 for x18 devices.
4. A_0–A_{14} for 32K; A_0–A_{15} for 64K devices.
5. BUSY is an output in master mode and an input in slave mode.

Functional Description

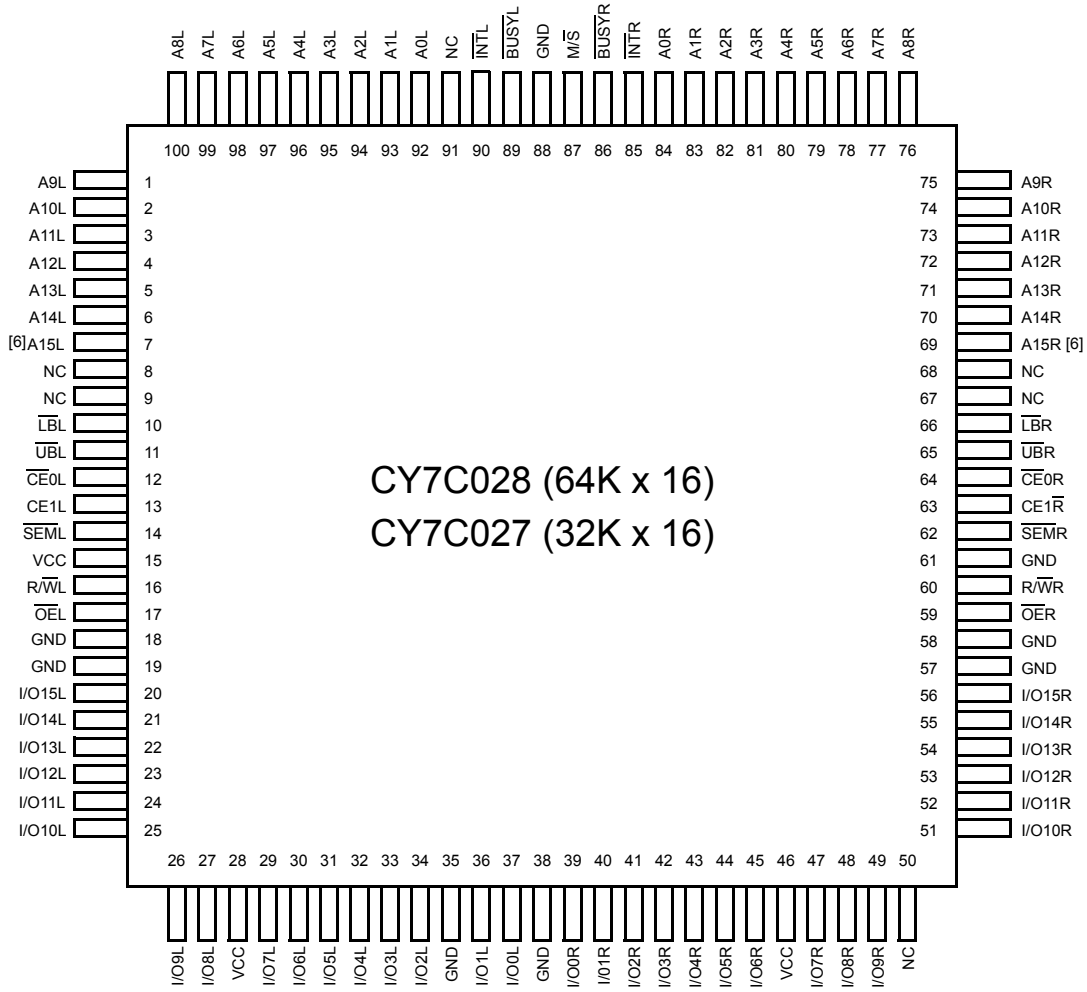
The CY7C027/028 and CY7C037/038 are low-power CMOS 32K, 64K x 16/18 dual-port static RAMs. Various arbitration schemes are included on the devices to handle situations when multiple processors access the same piece of data. Two ports are provided, permitting independent, asynchronous access for reads and writes to any location in memory. The devices can be utilized as standalone 16/18-bit dual-port static RAMs or multiple devices can be combined in order to function as a 32/36-bit or wider master/slave dual-port static RAM. An M/$\overline{S}$ pin is provided for implementing 32/36-bit or wider memory applications without the need for separate master and slave devices or additional discrete logic. Application areas include interprocessor/multiprocessor designs, communications status buffering, and dual-port video/graphics memory.

Each port has independent control pins: dual chip enables ($\overline{CE}_0$ and CE_1), read or write enable (R/$\overline{W}$), and output enable ($\overline{OE}$). Two flags are provided on each port ($\overline{BUSY}$ and $\overline{INT}$). $\overline{BUSY}$ signals that the port is trying to access the same location currently being accessed by the other port. The interrupt flag ($\overline{INT}$) permits communication between ports or systems by means of a mail box. The semaphores are used to pass a flag, or token, from one port to the other to indicate that a shared resource is in use. The semaphore logic is comprised of eight shared latches. Only one side can control the latch (semaphore) at any time. Control of a semaphore indicates that a shared resource is in use. An automatic power-down feature is controlled independently on each port by the chip enable pins.

The CY7C027/028 and CY7C037/038 are available in 100-pin Thin Quad Plastic Flatpack (TQFP) packages.

Pin Configurations

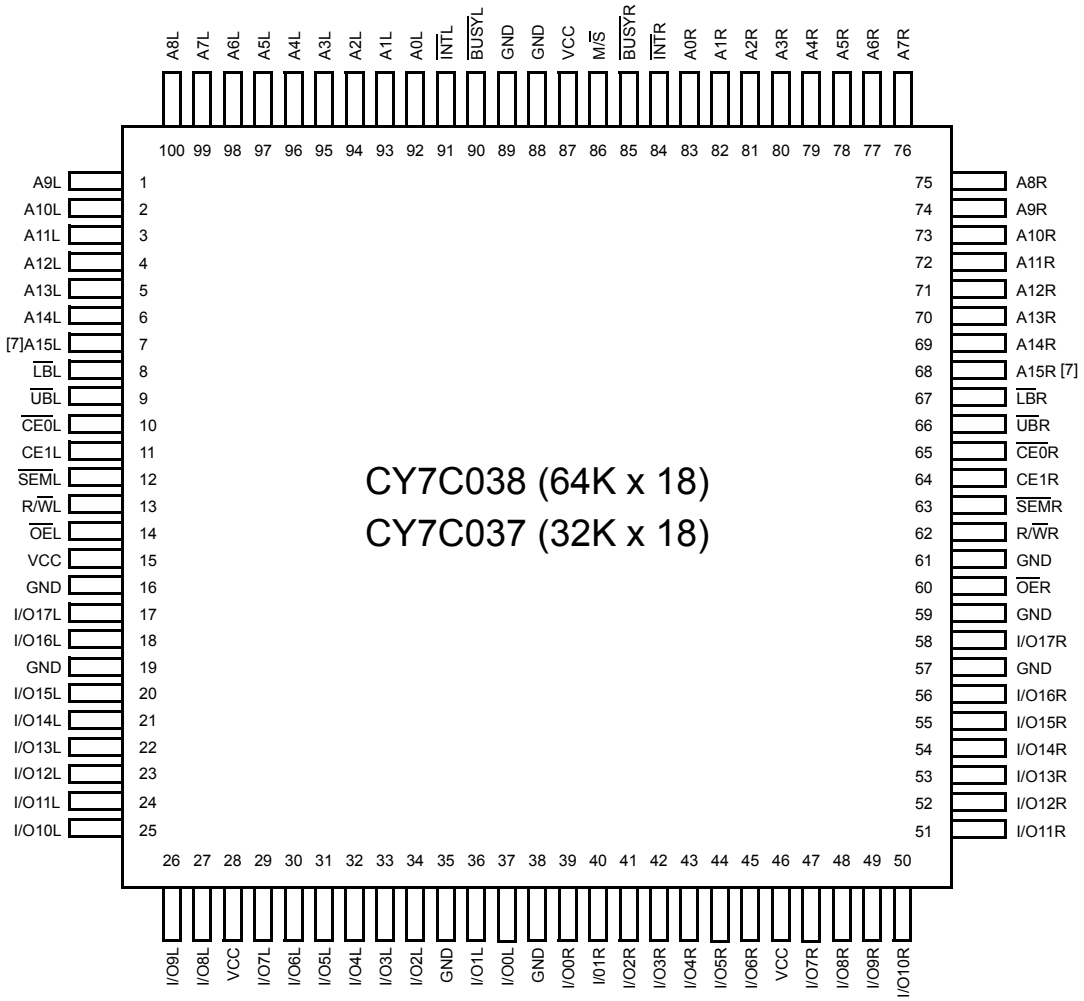
100-Pin TQFP (Top View)



Note:
6. This pin is NC for CY7C027.

Pin Configurations (continued)

100-Pin TQFP (Top View)



Selection Guide

	CY7C027/028 CY7C037/038 -12[1]	CY7C027/028 CY7C037/038 -15	CY7C027/028 CY7C037/038 -20	Unit
Maximum Access Time	12	15	20	ns
Typical Operating Current	195	190	180	mA
Typical Standby Current for I_{SB1} (Both ports TTL level)	55	50	45	mA
Typical Standby Current for I_{SB3} (Both ports CMOS level)	0.05	0.05	0.05	mA

Note:
7. This pin is NC for CY7C037.

Pin Definitions

Left Port	Right Port	Description
$\overline{CE}_{0L}$, CE_{1L}	$\overline{CE}_{0R}$, CE_{1R}	Chip Enable ($\overline{CE}$ is LOW when $\overline{CE}_0 \le V_{IL}$ and $CE_1 \ge V_{IH}$)
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
A_{0L}–A_{15L}	A_{0R}–A_{15R}	Address (A_0–A_{14} for 32K; A_0–A_{15} for 64K devices)
I/O_{0L}–I/O_{17L}	I/O_{0R}–I/O_{17R}	Data Bus Input/Output (I/O_0–I/O_{15} for x16 devices; I/O_0–I/O_{17} for x18)
$\overline{SEM}_L$	$\overline{SEM}_R$	Semaphore Enable
$\overline{UB}_L$	$\overline{UB}_R$	Upper Byte Select (I/O_8–I/O_{15} for x16 devices; I/O_9–I/O_{17} for x18 devices)
$\overline{LB}_L$	$\overline{LB}_R$	Lower Byte Select (I/O_0–I/O_7 for x16 devices; I/O_0–I/O_8 for x18 devices)
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
$M/\overline{S}$		Master or Slave Select
V_{CC}		Power
GND		Ground
NC		No Connect

Maximum Ratings[8]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage to Ground Potential ..... –0.3V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... –0.5V to +7.0DC

Input Voltage[9] ..... –0.5V to +7.0V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... >1100V

Latch-Up Current..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial[10]	–40°C to +85°C	5V ± 10%

Notes:
8. The Voltage on any input or I/O pin cannot exceed the power pin during power-up.
9. Pulse width < 20 ns.
10. Industrial parts are available in CY7C028 and CY7C038 only.

Electrical Characteristics Over the Operating Range

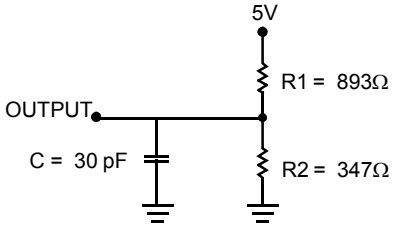
Symbol	Parameter		CY7C027/028 CY7C037/038									Unit
			-12[1]			-15			-20			
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{OH}	Output HIGH Voltage (V_{CC} = Min., I_{OH} = –4.0 mA)		2.4			2.4			2.4			V
V_{OL}	Output LOW Voltage (V_{CC} = Min., I_{OH} = +4.0 mA)				0.4			0.4			0.4	V
V_{IH}	Input HIGH Voltage		2.2			2.2			2.2			V
V_{IL}	Input LOW Voltage				0.8			0.8			0.8	V
I_{OZ}	Output Leakage Current		–10		10	–10		10	–10		10	μA
I_{CC}	Operating Current (V_{CC}=Max, I_{OUT}=0 mA) Outputs Disabled	Com'l.		195	325		190	280		180	265	mA
		Ind.[10]								305	290	mA
I_{SB1}	Standby Current (Both Ports TTL Level) $\overline{CE}_L$ & $\overline{CE}_R \geq V_{IH}$, f = f_{MAX}	Com'l.		55	75		50	70		45	65	mA
		Ind.[10]								60	80	mA
I_{SB2}	Standby Current (One Port TTL Level) $\overline{CE}_L$ | $\overline{CE}_R \geq V_{IH}$, f = f_{MAX}	Com'l.		125	205		120	180		110	160	mA
		Ind.[10]								125	175	mA
I_{SB3}	Standby Current (Both Ports CMOS Level) $\overline{CE}_L$ & $\overline{CE}_R \geq V_{CC}$ – 0.2V, f = 0	Com'l.		0.05	0.5		0.05	0.5		0.05	0.5	mA
		Ind.[10]								0.05	0.5	mA
I_{SB4}	Standby Current (One Port CMOS Level) $\overline{CE}_L$ | $\overline{CE}_R \geq V_{IH}$, f = f_{MAX}[11]	Com'l.		115	185		110	160		100	140	mA
		Ind.[10]								115	155	mA

Capacitance[12]

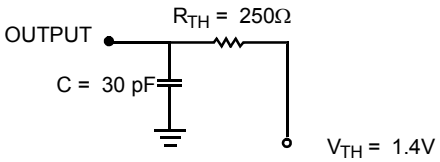
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Note:
11. $f_{MAX} = 1/t_{RC}$ = All inputs cycling at f = $1/t_{RC}$ (except output enable). f = 0 means no address or control lines change. This applies only to inputs at CMOS level standby I_{SB3}

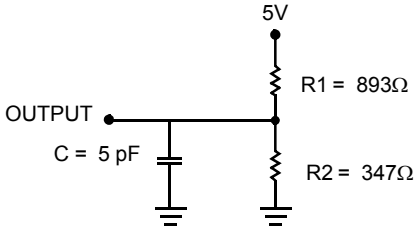
AC Test Loads and Waveforms



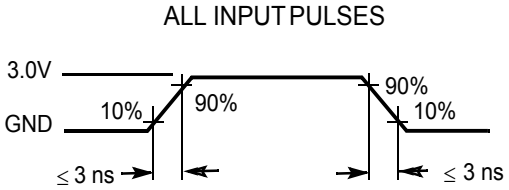
(a) Normal Load (Load 1)



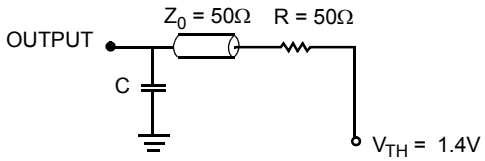
(b) Thévenin Equivalent (Load 1)



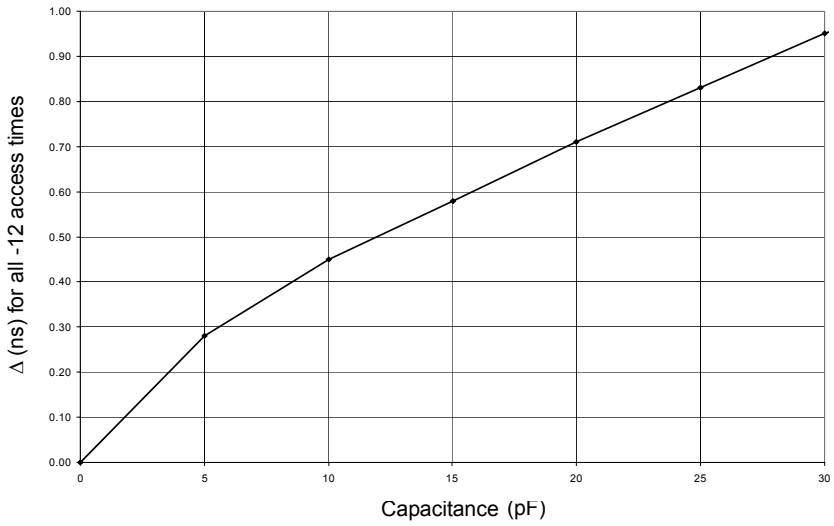
(c) Three-State Delay (Load 2)
(Used for t_{CKLZ}, t_{OLZ}, & t_{OHZ} including scope and jig)



AC Test Loads (Applicable to -12 only)[13]



(a) Load 1 (-12 only)



(b) Load Derating Curve

Notes:
12. Tested initially and after any design or process changes that may affect these parameters.
13. Test Conditions: C = 0 pF.

Switching Characteristics Over the Operating Range[14]

Parameter	Description	CY7C027/028 CY7C037/038						Unit
		-12[1]		-15		-20		
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	12		15		20		ns
t_{AA}	Address to Data Valid		12		15		20	ns
t_{OHA}	Output Hold From Address Change	3		3		3		ns
t_{ACE}[15]	$\overline{CE}$ LOW to Data Valid		12		15		20	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		8		10		12	ns
t_{LZOE}[16, 17, 18]	$\overline{OE}$ LOW to Low Z	3		3		3		ns
t_{HZOE}[16, 17, 18]	$\overline{OE}$ HIGH to High Z		10		10		12	ns
t_{LZCE}[16, 17, 18]	$\overline{CE}$ LOW to Low Z	3		3		3		ns
t_{HZCE}[16, 17, 18]	$\overline{CE}$ HIGH to High Z		10		10		12	ns
t_{PU}[18]	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t_{PD}[18]	$\overline{CE}$ HIGH to Power-Down		12		15		20	ns
t_{ABE}[15]	Byte Enable Access Time		12		15		20	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	12		15		20		ns
t_{SCE}[15]	$\overline{CE}$ LOW to Write End	10		12		15		ns
t_{AW}	Address Valid to Write End	10		12		15		ns
t_{HA}	Address Hold From Write End	0		0		0		ns
t_{SA}[15]	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	Write Pulse Width	10		12		15		ns
t_{SD}	Data Set-Up to Write End	10		10		15		ns
t_{HD}	Data Hold From Write End	0		0		0		ns
t_{HZWE}[17, 18]	R/$\overline{W}$ LOW to High Z		10		10		12	ns
t_{LZWE}[17, 18]	R/$\overline{W}$ HIGH to Low Z	3		3		3		ns
t_{WDD}[19]	Write Pulse to Data Delay		25		30		45	ns
t_{DDD}[19]	Write Data Valid to Read Data Valid		20		25		30	ns
BUSY TIMING[20]								
t_{BLA}	$\overline{BUSY}$ LOW from Address Match		12		15		20	ns
t_{BHA}	$\overline{BUSY}$ HIGH from Address Mismatch		12		15		20	ns
t_{BLC}	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW		12		15		20	ns
t_{BHC}	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH		12		15		17	ns
t_{PS}	Port Set-Up for Priority	5		5		5		ns
t_{WB}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ (Slave)	0		0		0		ns

Notes:
14. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
15. To access RAM, $\overline{CE}$=L, $\overline{UB}$=L, $\overline{SEM}$=H. To access semaphore, $\overline{CE}$=H and $\overline{SEM}$=L. Either condition must be valid for the entire t_{SCE} time.
16. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
17. Test conditions used are Load 2.
18. This parameter is guaranteed by design, but it is not production tested.
19. For information on port-to-port delay through RAM cells from writing port to reading port, refer to Read Timing with Busy waveform.
20. Test conditions used are Load 1.

Switching Characteristics Over the Operating Range[14] (continued)

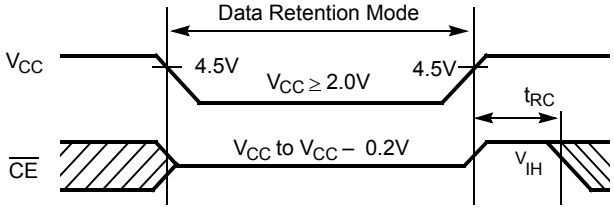
Parameter	Description	CY7C027/028 CY7C037/038						Unit
		-12[1]		-15		-20		
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{WH}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ HIGH (Slave)	11		13		15		ns
t_{BDD}[21]	$\overline{BUSY}$ HIGH to Data Valid		12		15		20	ns
INTERRUPT TIMING[20]								
t_{INS}	$\overline{INT}$ Set Time		12		15		20	ns
t_{INR}	$\overline{INT}$ Reset Time		12		15		20	ns
SEMAPHORE TIMING								
t_{SOP}	SEM Flag Update Pulse ($\overline{OE}$ or $\overline{SEM}$)	10		10		10		ns
t_{SWRD}	SEM Flag Write to Read Time	5		5		5		ns
t_{SPS}	SEM Flag Contention Window	5		5		5		ns
t_{SAA}	SEM Address Access Time		12		15		20	ns

Data Retention Mode

The CY7C027/028 and CY7C037/038 are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules ensure data retention:

1. Chip enable ($\overline{CE}$) must be held HIGH during data retention, within V_{CC} to V_{CC} – 0.2V.
2. $\overline{CE}$ must be kept between V_{CC} – 0.2V and 70% of V_{CC} during the power-up and power-down transitions.
3. The RAM can begin operation >t_{RC} after V_{CC} reaches the minimum operating voltage (4.5 volts).

Timing

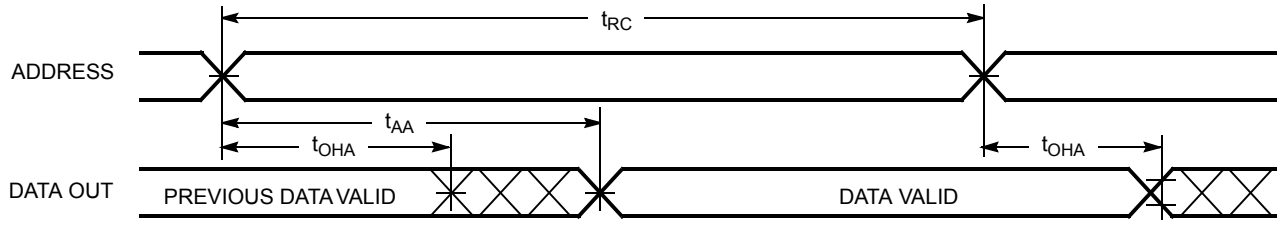


Parameter	Test Conditions[22]	Max.	Unit
ICC_{DR1}	@ VCC_{DR} = 2V	1.5	mA

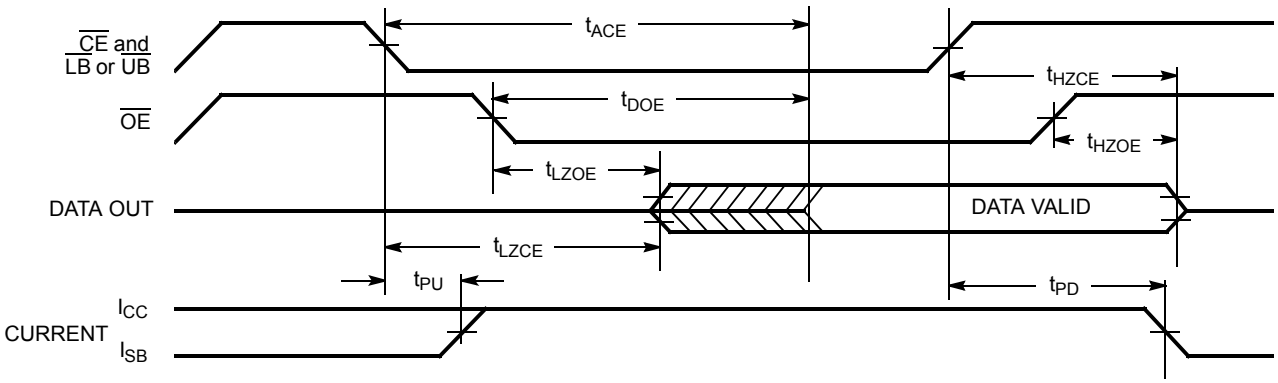
Notes:
21. t_{BDD} is a calculated parameter and is the greater of t_{WDD}–t_{PWE} (actual) or t_{DDD}–t_{SD} (actual).
22. $\overline{CE}$ = V_{CC}, V_{in} = GND to V_{CC}, T_A = 25°C. This parameter is guaranteed but not tested.

Switching Waveforms

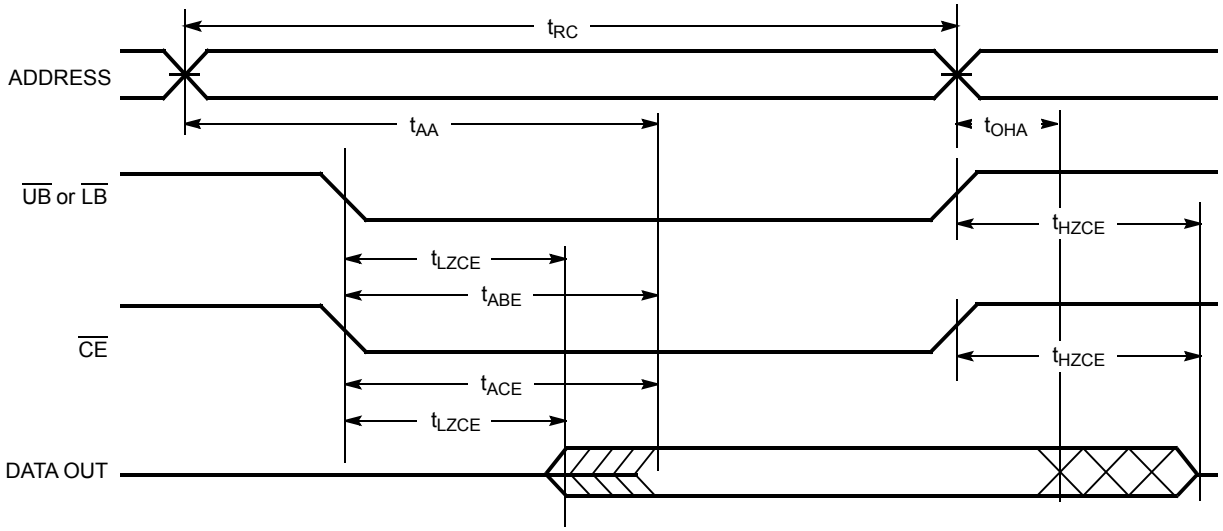
Read Cycle No. 1 (Either Port Address Access)[23 ,24, 25]



Read Cycle No. 2 (Either Port $\overline{CE}$/$\overline{OE}$ Access)[23, 26, 27]



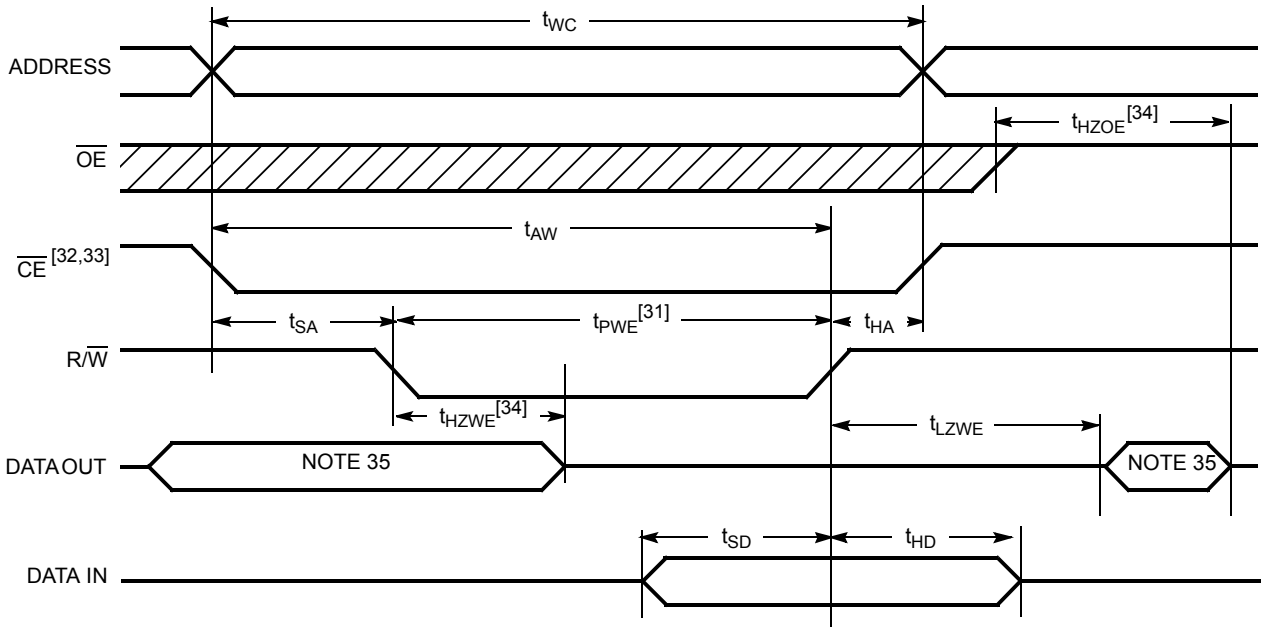
Read Cycle No. 3 (Either Port)[23, 25, 26, 27]



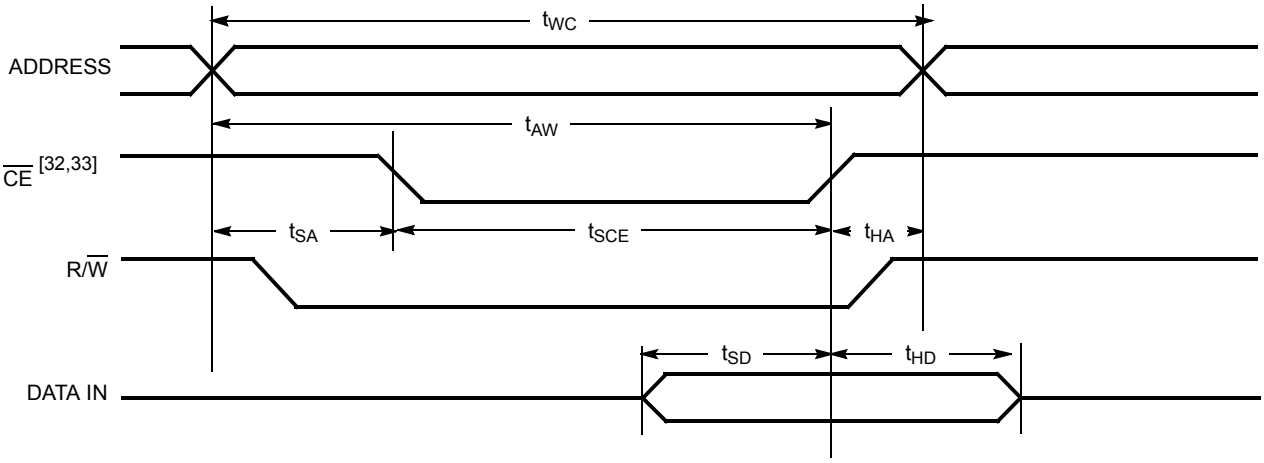
Notes:
23. R/$\overline{W}$ is HIGH for read cycles.
24. Device is continuously selected $\overline{CE}$ = V_{IL} and $\overline{UB}$ or $\overline{LB}$ = V_{IL}. This waveform cannot be used for semaphore reads.
25. $\overline{OE}$ = V_{IL}.
26. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
27. To access RAM, $\overline{CE}$ = V_{IL}, $\overline{UB}$ or $\overline{LB}$ = V_{IL}, $\overline{SEM}$ = V_{IH}. To access semaphore, $\overline{CE}$ = V_{IH}, $\overline{SEM}$ = V_{IL}.

Switching Waveforms (continued)

Write Cycle No. 1: R/$\overline{W}$ Controlled Timing[28, 29, 30, 31]



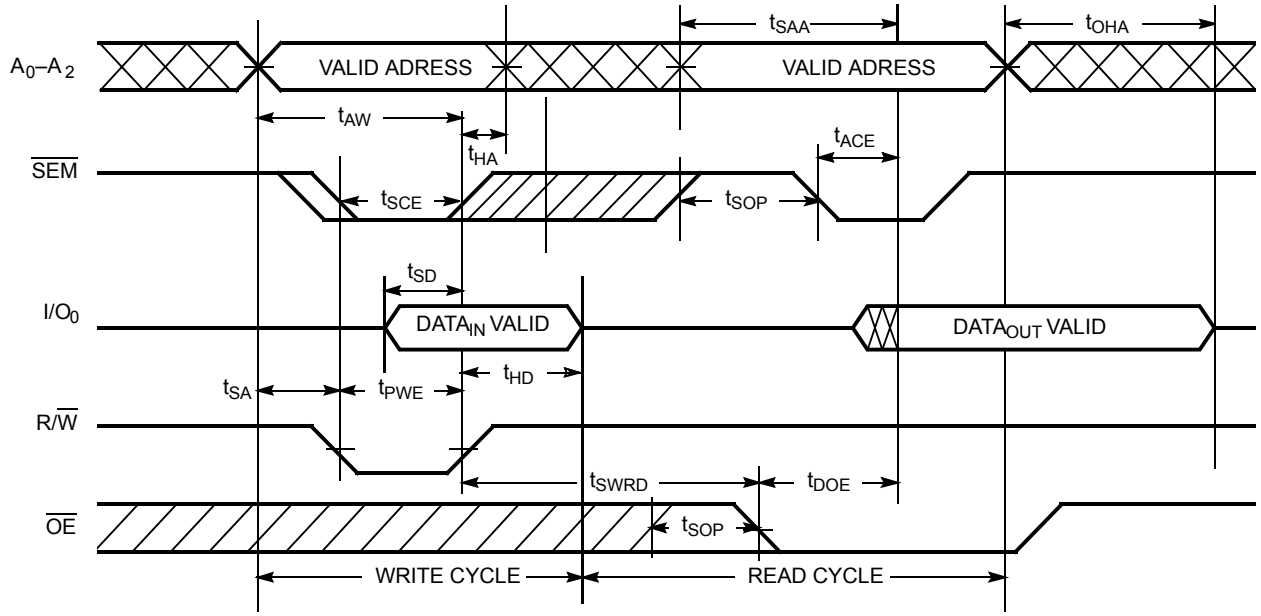
Write Cycle No. 2: $\overline{CE}$ Controlled Timing[28, 29, 30, 34, 35]



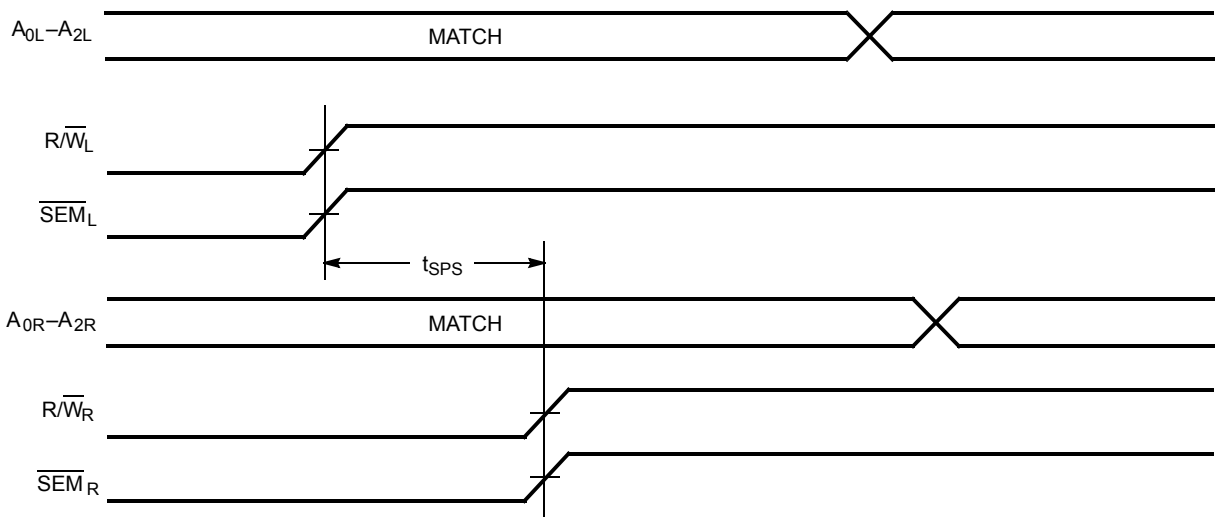
Notes:
28. R/$\overline{W}$ must be HIGH during all address transitions.
29. A write occurs during the overlap (t_{SCE} or t_{PWE}) of a LOW $\overline{CE}$ or $\overline{SEM}$ and a LOW $\overline{UB}$ or $\overline{LB}$.
30. t_{HA} is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ or ($\overline{SEM}$ or R/$\overline{W}$) going HIGH at the end of write cycle.
31. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{PWE} or (t_{HZWE} + t_{SD}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{SD}. If $\overline{OE}$ is HIGH during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{PWE}.
32. To access RAM, $\overline{CE}$ = V_{IL}, $\overline{SEM}$ = V_{IH}.
33. To access upper byte, $\overline{CE}$ = V_{IL}, $\overline{UB}$ = V_{IL}, $\overline{SEM}$ = V_{IH}.
    To access lower byte, $\overline{CE}$ = V_{IL}, $\overline{LB}$ = V_{IL}, $\overline{SEM}$ = V_{IH}.
34. Transition is measured ±500 mV from steady state with a 5-pF load (including scope and jig). This parameter is sampled and not 100% tested.
35. During this period, the I/O pins are in the output state, and input signals must not be applied.
36. If the $\overline{CE}$ or $\overline{SEM}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in the high-impedance state.

Switching Waveforms (continued)

Semaphore Read After Write Timing, Either Side[37]



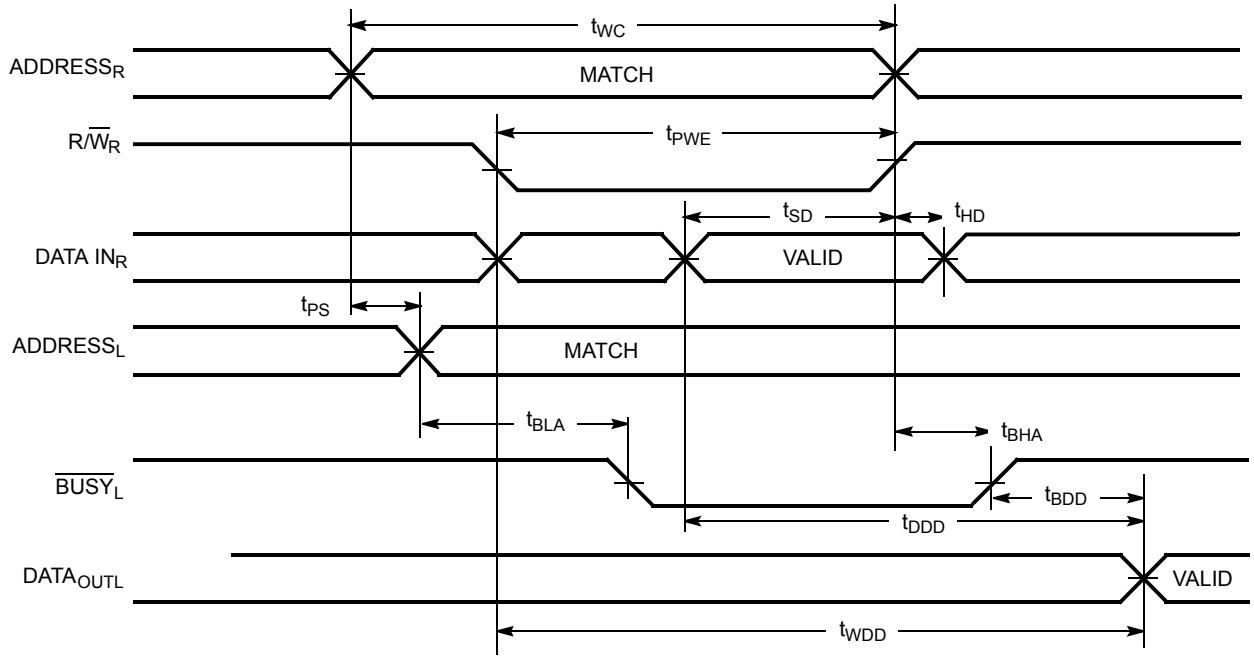
Timing Diagram of Semaphore Contention[38, 39, 40]



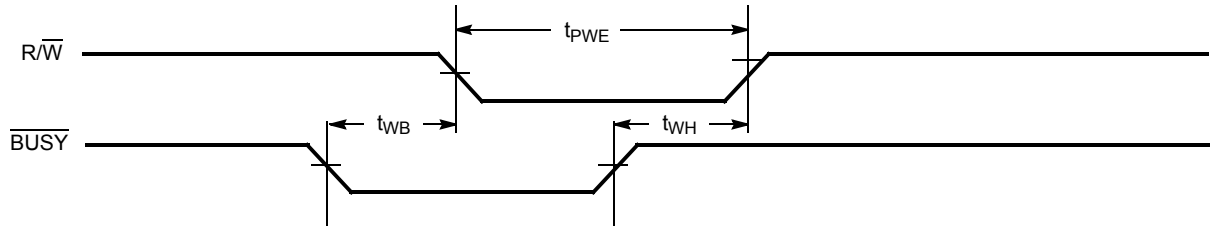
Notes:
37. $\overline{CE}$ = HIGH for the duration of the above timing (both write and read cycle).
38. $I/O_{0R} = I/O_{0L}$ = LOW (request semaphore); $\overline{CE}_R = \overline{CE}_L$ = HIGH.
39. Semaphores are reset (available to both ports) at cycle start.
40. If t_{SPS} is violated, the semaphore will definitely be obtained by one side or the other, but which side will get the semaphore is unpredictable.

Switching Waveforms (continued)

Timing Diagram of Read with $\overline{BUSY}$ (M/$\overline{S}$=HIGH)[41]



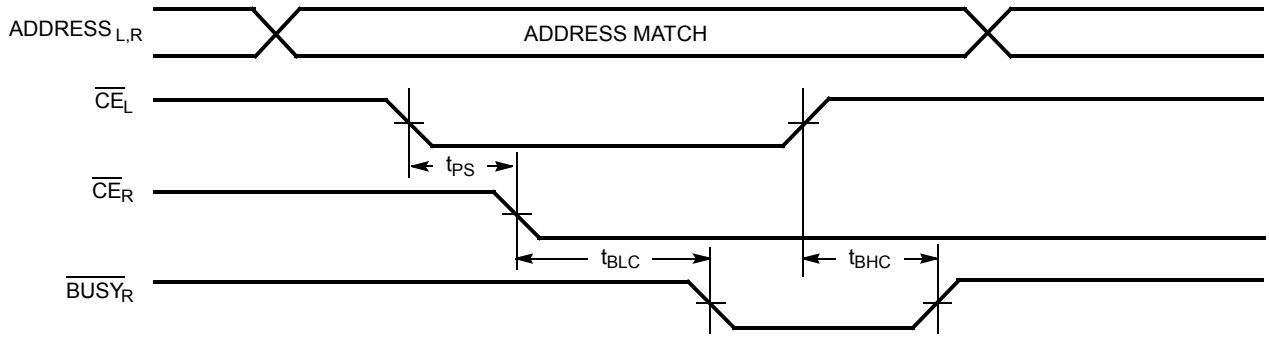
Write Timing with Busy Input (M/$\overline{S}$=LOW)



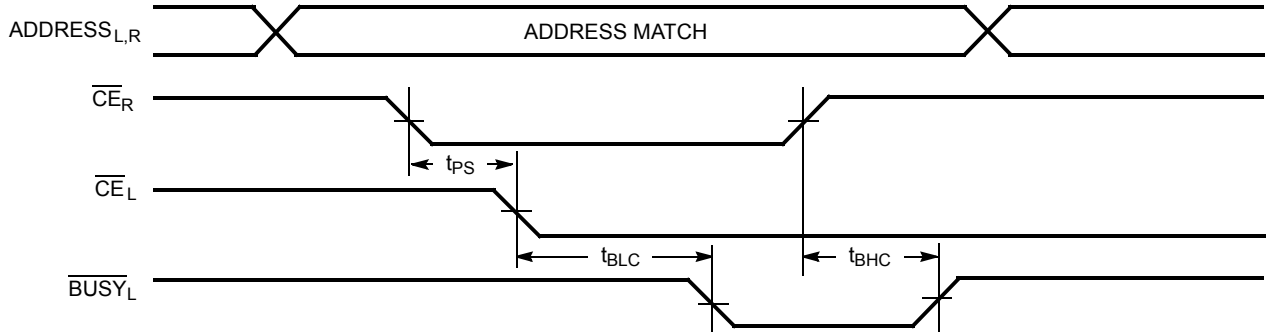
Note:
41. $\overline{CE}_L$ = $\overline{CE}_R$ = LOW.

Switching Waveforms (continued)

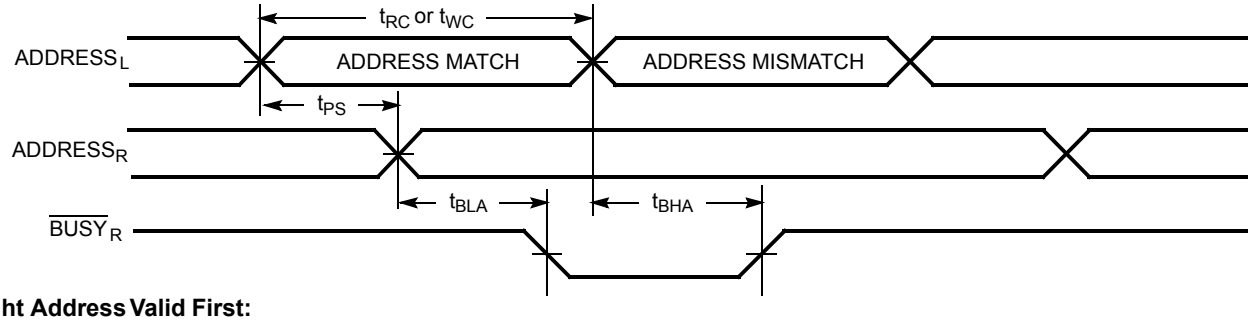
Busy Timing Diagram No.1 ($\overline{CE}$ Arbitration)[42]
CE_L Valid First:



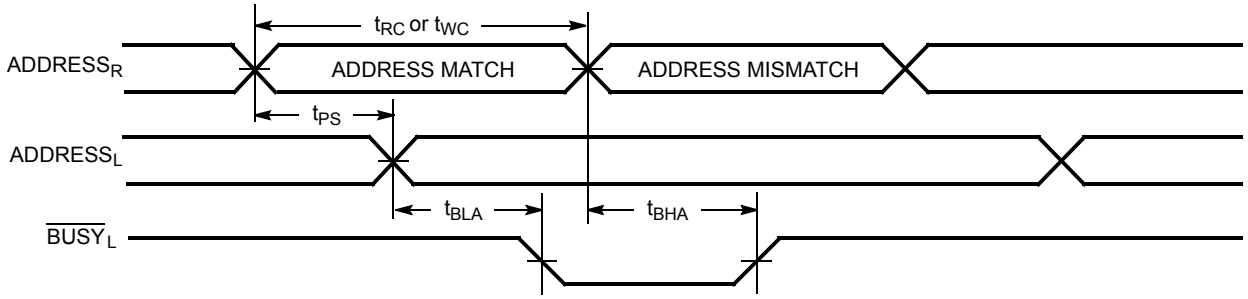
$\overline{CE}_R$ Valid First:



Busy Timing Diagram No. 2 (Address Arbitration)[42]
Left Address Valid First:



Right Address Valid First:

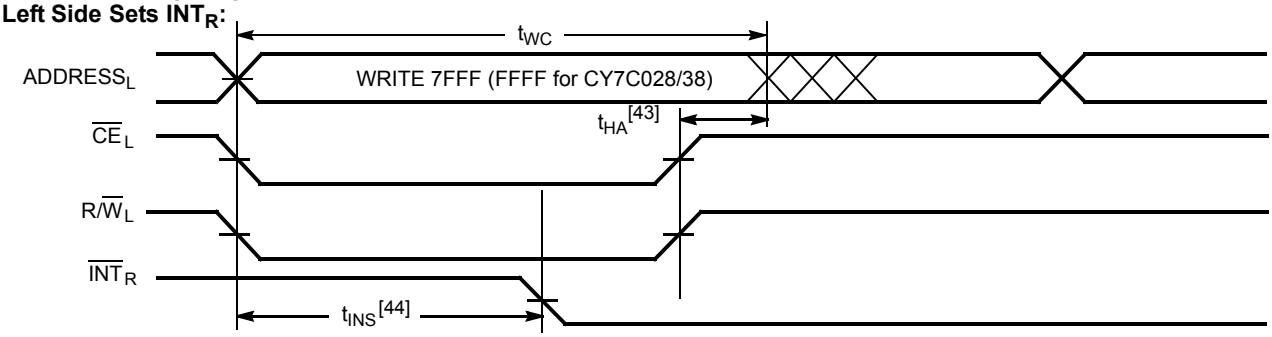


Note:
42. If t_{PS} is violated, the busy signal will be asserted on one side or the other, but there is no guarantee to which side $\overline{BUSY}$ will be asserted.

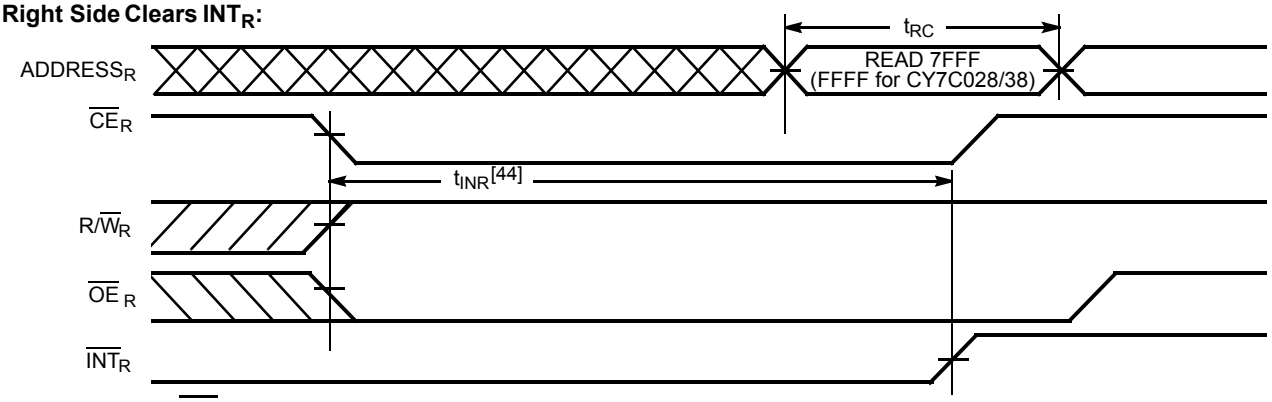
Switching Waveforms (continued)

Interrupt Timing Diagrams

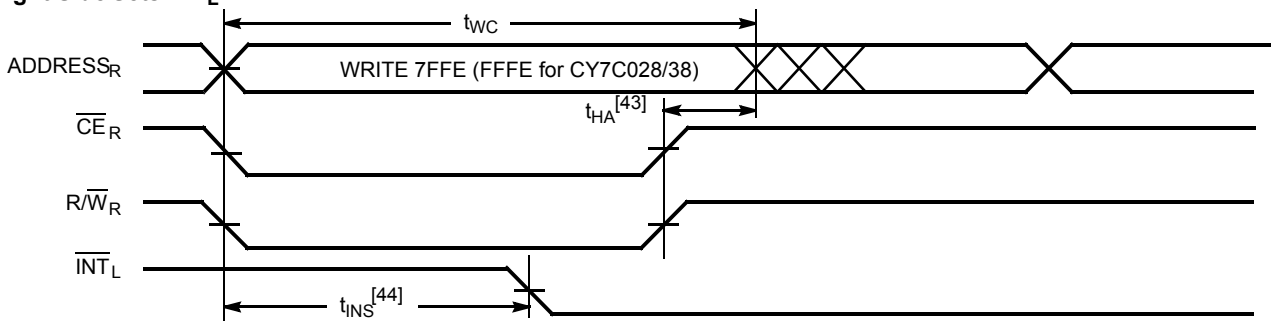
Left Side Sets $\overline{INT}_R$:



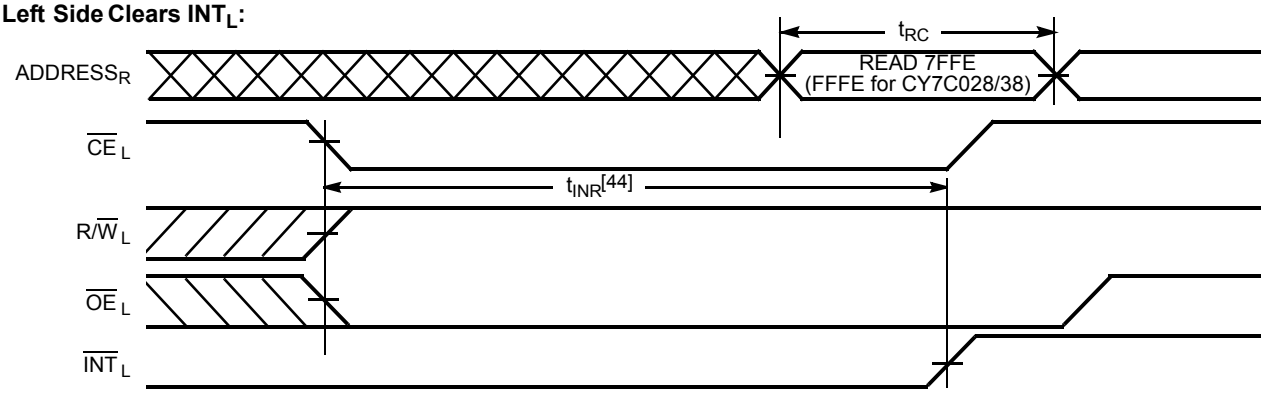
Right Side Clears $\overline{INT}_R$:



Right Side Sets $\overline{INT}_L$:



Left Side Clears $\overline{INT}_L$:



Notes:
43. t_{HA} depends on which enable pin ($\overline{CE}_L$ or $R/\overline{W}_L$) is deasserted first.
44. t_{INS} or t_{INR} depends on which enable pin ($\overline{CE}_L$ or $R/\overline{W}_L$) is asserted last.

Architecture

The CY7C027/028 and CY7C037/038 consist of an array of 32K and 64K words of 16 and 18 bits each of dual-port RAM cells, I/O and address lines, and control signals (CE, OE, R/W). These control pins permit independent access for reads or writes to any location in memory. To handle simultaneous writes/reads to the same location, a BUSY pin is provided on each port. Two interrupt (INT) pins can be utilized for port-to-port communication. Two semaphore (SEM) control pins are used for allocating shared resources. With the M/S pin, the devices can function as a master (BUSY pins are outputs) or as a slave (BUSY pins are inputs). The devices also have an automatic power-down feature controlled by CE. Each port is provided with its own output enable control (OE), which allows data to be read from the device.

Functional Description

Write Operation

Data must be set up for a duration of t_{SD} before the rising edge of R/W in order to guarantee a valid write. A write operation is controlled by either the R/W pin (see Write Cycle No. 1 waveform) or the CE pin (see Write Cycle No. 2 waveform). Required inputs for non-contention operations are summarized in *Table 1*.

If a location is being written to by one port and the opposite port attempts to read that location, a port-to-port flowthrough delay must occur before the data is read on the output; otherwise the data read is not deterministic. Data will be valid on the port t_{DDD} after the data is presented on the other port.

Read Operation

When reading the device, the user must assert both the OE and CE pins. Data will be available t_{ACE} after CE or t_{DOE} after OE is asserted. If the user wishes to access a semaphore flag, then the SEM pin must be asserted instead of the CE pin, and OE must also be asserted.

Interrupts

The upper two memory locations may be used for message passing. The highest memory location (7FFF for the CY7C027/37, FFFF for the CY7C028/38) is the mailbox for the right port and the second-highest memory location (7FFE for the CY7C027/37, FFFE for the CY7C028/38) is the mailbox for the left port. When one port writes to the other port's mailbox, an interrupt is generated to the owner. The interrupt is reset when the owner reads the contents of the mailbox. The message is user defined.

Each port can read the other port's mailbox without resetting the interrupt. The active state of the busy signal (to a port) prevents the port from setting the interrupt to the winning port. Also, an active busy to a port prevents that port from reading its own mailbox and, thus, resetting the interrupt to it.

If an application does not require message passing, do not connect the interrupt pin to the processor's interrupt request input pin.

The operation of the interrupts and their interaction with Busy is summarized in *Table 2.*

Busy

The CY7C027/028 and CY7C037/038 provide on-chip arbitration to resolve simultaneous memory location access (contention). If both ports' CEs are asserted and an address match occurs within t_{PS} of each other, the busy logic will determine which port has access. If t_{PS} is violated, one port will definitely gain permission to the location, but it is not predictable which port will get that permission. BUSY will be asserted t_{BLA} after an address match or t_{BLC} after CE is taken LOW.

Master/Slave

A M/S pin is provided in order to expand the word width by configuring the device as either a master or a slave. The BUSY output of the master is connected to the BUSY input of the slave. This will allow the device to interface to a master device with no external components. Writing to slave devices must be delayed until after the BUSY input has settled (t_{BLC} or t_{BLA}), otherwise, the slave chip may begin a write cycle during a contention situation. When tied HIGH, the M/S pin allows the device to be used as a master and, therefore, the BUSY line is an output. BUSY can then be used to send the arbitration outcome to a slave.

Semaphore Operation

The CY7C027/028 and CY7C037/038 provide eight semaphore latches, which are separate from the dual-port memory locations. Semaphores are used to reserve resources that are shared between the two ports.The state of the semaphore indicates that a resource is in use. For example, if the left port wants to request a given resource, it sets a latch by writing a zero to a semaphore location. The left port then verifies its success in setting the latch by reading it. After writing to the semaphore, SEM or OE must be deasserted for t_{SOP} before attempting to read the semaphore. The semaphore value will be available $t_{SWRD} + t_{DOE}$ after the rising edge of the semaphore write. If the left port was successful (reads a zero), it assumes control of the shared resource, otherwise (reads a one) it assumes the right port has control and continues to poll the semaphore. When the right side has relinquished control of the semaphore (by writing a one), the left side will succeed in gaining control of the semaphore. If the left side no longer requires the semaphore, a one is written to cancel its request.

Semaphores are accessed by asserting SEM LOW. The SEM pin functions as a chip select for the semaphore latches (CE must remain HIGH during SEM LOW). A_{0-2} represents the semaphore address. OE and R/W are used in the same manner as a normal memory access. When writing or reading a semaphore, the other address pins have no effect.

When writing to the semaphore, only I/O_0 is used. If a zero is written to the left port of an available semaphore, a one will appear at the same semaphore address on the right port. That semaphore can now only be modified by the side showing zero (the left port in this case). If the left port now relinquishes control by writing a one to the semaphore, the semaphore will be set to one for both sides. However, if the right port had requested the semaphore (written a zero) while the left port had control, the right port would immediately own the semaphore as soon as the left port released it. *Table 3* shows sample semaphore operations.

When reading a semaphore, all sixteen/eighteen data lines output the semaphore value. The read value is latched in an output register to prevent the semaphore from changing state during a write from the other port. If both ports attempt to access the semaphore within t_{SPS} of each other, the semaphore will definitely be obtained by one side or the other, but there is no guarantee which side will control the semaphore.

Table 1. Non-Contending Read/Write

Inputs						Outputs		
$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	$\overline{UB}$	$\overline{LB}$	$\overline{SEM}$	I/O_9–I/O_{17}	I/O_0–I/O_8	Operation
H	X	X	X	X	H	High Z	High Z	Deselected: Power-Down
X	X	X	H	H	H	High Z	High Z	Deselected: Power-Down
L	L	X	L	H	H	Data In	High Z	Write to Upper Byte Only
L	L	X	H	L	H	High Z	Data In	Write to Lower Byte Only
L	L	X	L	L	H	Data In	Data In	Write to Both Bytes
L	H	L	L	H	H	Data Out	High Z	Read Upper Byte Only
L	H	L	H	L	H	High Z	Data Out	Read Lower Byte Only
L	H	L	L	L	H	Data Out	Data Out	Read Both Bytes
X	X	H	X	X	X	High Z	High Z	Outputs Disabled
H	H	L	X	X	L	Data Out	Data Out	Read Data in Semaphore Flag
X	H	L	H	H	L	Data Out	Data Out	Read Data in Semaphore Flag
H	⎍	X	X	X	L	Data In	Data In	Write D_{IN0} into Semaphore Flag
X	⎍	X	H	H	L	Data In	Data In	Write D_{IN0} into Semaphore Flag
L	X	X	L	X	L			Not Allowed
L	X	X	X	L	L			Not Allowed

Table 2. Interrupt Operation Example (assumes $\overline{BUSY}_L$ = $\overline{BUSY}_R$ = HIGH)[45]

	Left Port					Right Port				
Function	R/$\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	$A_{0L–14L}$	$\overline{INT}_L$	R/$\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	$A_{0R–14R}$	$\overline{INT}_R$
Set Right $\overline{INT}_R$ Flag	L	L	X	7FFF	X	X	X	X	X	L[47]
Reset Right $\overline{INT}_R$ Flag	X	X	X	X	X	X	L	L	7FFF	H[46]
Set Left $\overline{INT}_L$ Flag	X	X	X	X	L[46]	L	L	X	7FFE	X
Reset Left $\overline{INT}_L$ Flag	X	L	L	7FFE	H[47]	X	X	X	X	X

Notes:
45. $A_{0L–15L}$ and $A_{0R–15R}$, FFFF/FFFE for the CY7C028/038.
46. If $\overline{BUSY}_R$ = L, then no change.
47. If $\overline{BUSY}_L$ = L, then no change.

Table 3. Semaphore Operation Example

Function	I/O_0–I/O_{17} Left	I/O_0–I/O_{17} Right	Status
No action	1	1	Semaphore free
Left port writes 0 to semaphore	0	1	Left Port has semaphore token
Right port writes 0 to semaphore	0	1	No change. Right side has no write access to semaphore
Left port writes 1 to semaphore	1	0	Right port obtains semaphore token
Left port writes 0 to semaphore	1	0	No change. Left port has no write access to semaphore
Right port writes 1 to semaphore	0	1	Left port obtains semaphore token
Left port writes 1 to semaphore	1	1	Semaphore free
Right port writes 0 to semaphore	1	0	Right port has semaphore token
Right port writes 1 to semaphore	1	1	Semaphore free
Left port writes 0 to semaphore	0	1	Left port has semaphore token
Left port writes 1 to semaphore	1	1	Semaphore free

Ordering Information

32K x16 Asynchronous Dual-Port SRAM

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12[1]	CY7C027-12AC	A100	100-Pin Thin Quad Flat Pack	Commercial
15	CY7C027-15AC	A100	100-Pin Thin Quad Flat Pack	Commercial
20	CY7C027-20AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C027-20AXC	A100	100-Pin Pb-Free Thin Quad Flat Pack	Commercial

64K x16 Asynchronous Dual-Port SRAM

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12[1]	CY7C028-12AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C028-12AXC	A100	100-Pin Pb-Free Thin Quad Flat Pack	Commercial
15	CY7C028-15AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C028-15AXC	A100	100-Pin Pb-Free Thin Quad Flat Pack	Commercial
	CY7C028-15AI	A100	100-Pin Thin Quad Flat Pack	Industrial
	CY7C028-15AXI	A100	100-Pin Pb-Free Thin Quad Flat Pack	Industrial
20	CY7C028-20AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C028-20AI	A100	100-Pin Thin Quad Flat Pack	Industrial

32K x18 Asynchronous Dual-Port SRAM

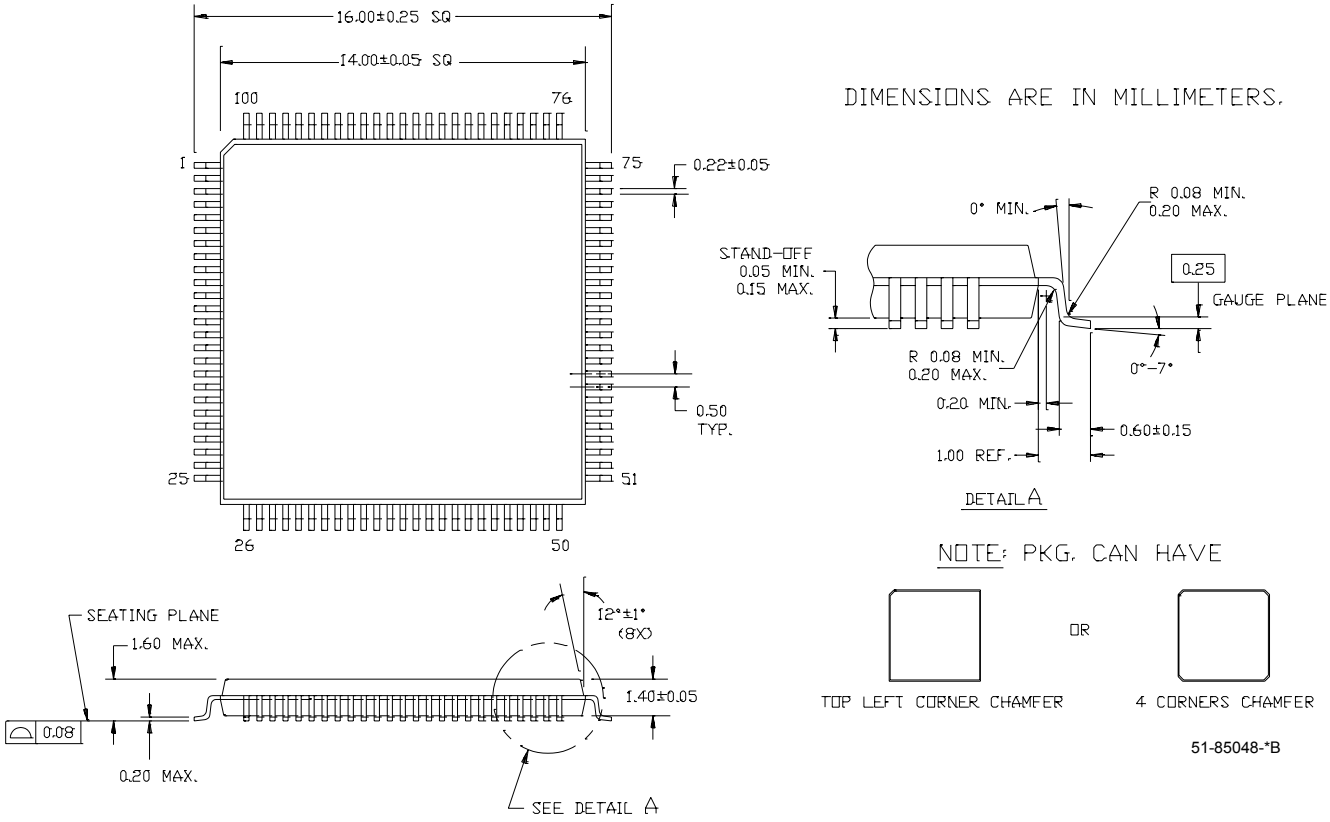
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12[1]	CY7C037-12AC	A100	100-Pin Thin Quad Flat Pack	Commercial
15	CY7C037-15AC	A100	100-Pin Thin Quad Flat Pack	Commercial
20	CY7C037-20AC	A100	100-Pin Thin Quad Flat Pack	Commercial

64K x18 Asynchronous Dual-Port SRAM

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12[1]	CY7C038-12AC	A100	100-Pin Thin Quad Flat Pack	Commercial
15	CY7C038-15AC	A100	100-Pin Thin Quad Flat Pack	Commercial
20	CY7C038-20AC	A100	100-Pin Thin Quad Flat Pack	Commercial
	CY7C038-20AI	A100	100-Pin Thin Quad Flat Pack	Industrial

Package Diagram

100-Pin Thin Plastic Quad Flat Pack (TQFP) A100
100-Pin Pb-Free Thin Plastic Quad Flat Pack (TQFP) A100



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Document History Page

Document Title: CY7C027/028, CY7C037/038 32K/64K x 16/18 Dual-Port Static RAM Document Number: 38-06042				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	110190	09/29/01	SZV	Change from Spec number: 38-00666 to 38-06042
*A	122292	12/27/02	RBI	Power up requirements added to Maximum Ratings Information
*B	236765	6/23/04	YDT	Removed cross information from features section
*C	377454	See ECN	PCX	Added Pb-Free Logo Added Pb-Free parts to ordering information: CY7C027-20AXC, CY7C028-12AXC, CY7C028-15AXC, CY7C028-15AI, CY7C028-15AXI